4-bit Ping-Pong Counter: PASS

First-In First Out (FIFO) Queue: PASS

Round-Robin FIFO Arbiter: PASS

4-bit Paramterized Ping-Pong Counter: PASS

Multi\_Bank\_Memory: FILE\_DNE

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Round-Robin FIFO Arbiter:

-IN your diagram, vaild should be one of output signal

Paramterized Ping-Pong Counter:

- Detailed explanation

FPGA:

- Complete & detailed circuit diagrams

- Need more explanation alongside the circuits

Take Away Part:

- I think the problem you have encountered might be resolved if you can use the system clock to trigger your DFFs, instead of using the divided clock.

- It is great that you have learned how to design sequential circuits and the concept of clock signals.

- Keep in mind that combinational and sequential circuits should be treated separately.